

Simplifying I2C Electrical Validation and Protocol Decode Using PGY-I2C Software

Overview of I2C Bus:

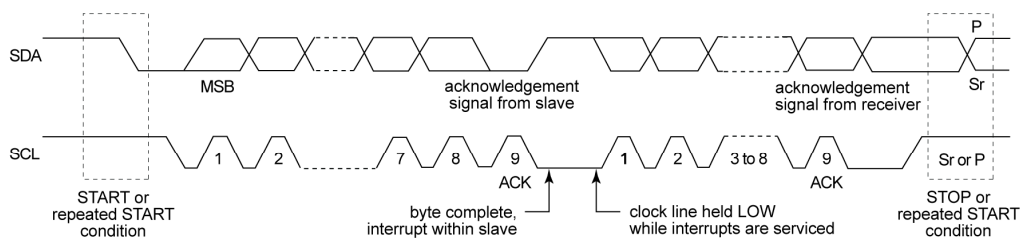
In early 1980s Philips Semiconductor developed a simple bidirectional 2-wire bus for efficient inter-IC control. This bus is called Inter IC or I2C bus. All I2C Bus compatible devices incorporate an on-chip interface which allows them to communicate directly with each other via the I2C –bus.

The I2C's physical two-wire interface consists of a bi-directional serial clock (SCL) and data (SDA) lines. Each device that is connected to the bus is software-addressable by a unique address and simple master/slave relationship with the bus exists all the time. I2C is a serial, 8-bit oriented, bi-directional data transfers can be made at 100Kbits/s in the standard mode, up to 400Kbits/s in the Fast mode, up to 1Mbits/s in fast Mode plus, or up to 3.4Mbits/s in the high speed mode. On-chip filtering rejects spikes on the bus data line to preserve data integrity.

Phillips Semiconductor (now NXP Semiconductors) has published electrical specifications and protocol specification since 1982. The recent I2C- bus specification and user manual was published in year 2007. By following the electrical and protocol specification in the I2C document, semiconductor design and manufacturing companies can ensure interoperability of ICs using I2C Bus.

I2C protocol overview:

Typical data transfer between two ICs using the I2C interface is as shown:



All transactions start with START Condition and stop with STOP condition In I2C Bus. These two conditions are controlled by the master IC. The typical I2C frame format has the following contents: START, address, read/write, data followed by ACK/NACK, and STOP condition at end of the operation.

START: A condition where high to low transition of SDA line occurs when SCL is held high. The is initiated by the master IC.

Address: Master sends the slave the 7- bit or 10- bit address of the slave device

Read/write: The slave address is followed by this bit. A ZERO indicates a transmission (write), and a 'ONE' indicates a request for READ.

Acknowledge (ACK) and Not Acknowledge (NACK): This takes place after every byte. During this condition the transmitter releases the SDA line during the acknowledge clock pulse so that the receiver can pull the SDA line LOW, and the SDA line remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this 9th clock pulse, this defined as the Not Acknowledgement signal. The master can then regenerate either a STOP condition to abort the transfer or a repeated START condition to start a new transfer.

Data is an integer number of bytes read or written into device.

STOP: A condition during SDA transitions from LOW to HIGH when SCL is held high indicating the end of transfer of data.

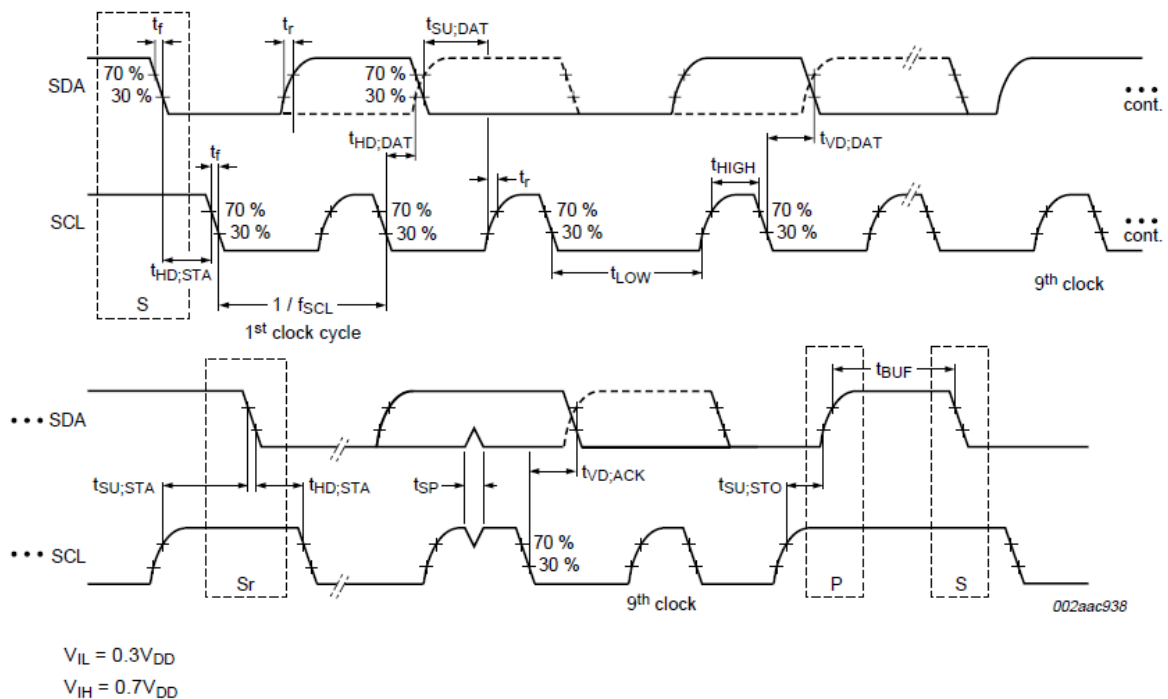
I2C Electrical Measurements:

For successful interoperation of IC using I2C bus, the electrical characteristics of physical layer signals of I2C SCL and SDA signals should be compatibility. The timing between the master and slave devices should be within electrical specifications defined in the I2C Specification by NXP Semiconductor. The electrical measurement list is as follows:

Symbol	Parameter	Symbol	Paramater
f_{SCL}	SCL Clock Frequency	t_r	rise time of both SDA and SCL Signals
$t_{HD;STA}$	hold time (repeated) START condition	t_f	fall time of both SDA and SCL signals
t_{LOW}	Low Period of the SCL clock	$t_{SU; STO}$	set-up time for STOP condition
t_{HIGH}	High Period of the SCL clock	t_{BUF}	bus free time between a STOP and START condition
$t_{SU;STA}$	set-up time for a repeated START condition	$t_{VD; DAT}$	data valid time
$t_{HD;DAT}$	Data hold time	$t_{VD; ACK}$	data valid acknowledge time
$t_{SU;DAT}$	Data setup time		

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The detailed definitions of each of these measurements are as below:



f_{SCL} SCL Clock frequency: Inverse of one cycle period measured at 30% of amplitude of SCL signal. It should be measured at first cycle of after the START condition.

t_r rise time of the SCL and SDA signals: time taken by rising edge to reach 70% of the amplitude from 30% of the amplitude of SCL and SDA signals.

t_f fall time of the SCL and SDA signals: time taken by the falling edge of the signals to reach 30% of the amplitude from 70% of the amplitude of SCL and SDA signals

$t_{HD,STA}$ hold time (repeated) START condition: Minimum time the data should be low before SCL is in low state at (repeated) START condition. It is measured as time taken from 30% of the amplitude of SDA at high to low transition to 70% of the amplitude at high to low transition of SCL Signal.

t_{LOW} Low period of the SCL signal: It is minimum low time that should be maintained by SCL signal. It is measured as half period measured at 30% of the amplitude of the SCL signal.

t_{HIGH} High period of the SCL Signal: It is minimum high time that should be maintained by SCL signal. It is measured as half period measured at 70% of the amplitude of SCL signal.

$t_{SU,STO}$ Setup time at STOP condition: It is measured at STOP condition of I2C frame. It is measured as time between 70% of the amplitude at rising edge of SCL signal to 30% of the amplitude of SDA signal at STOP condition.

$t_{SU;STA}$ Setup time for repeated START condition: This measurement is carried out at repeated START condition only. It is time measured between SCL and SDA signal at 70% amplitude of the signals.

$t_{VD; DAT}$ Data Valid time: Measured at every data and clock transition. This is measured with reference to 30% amplitude falling edge of SCL to 70% of rising edge or 30% of the falling edge of SDA signal. The I2C specification maximum allowed data valid time at different I2C speeds.

$t_{VD; ACK}$ data valid acknowledge time: Measured at acknowledgement bit. It is time from 30% of falling edge of eighth clock from start of data to 70% of the ack bit or 30% of the ack bit.

Electrical Measurement Challenges:

During electrical validation of I2C bus, test engineers need to ensure the I2C bus should comply with electrical parameters of I2C Bus. The challenges faced while electrical validation of I2C bus as follows:

- Test/Design Engineer must know I2C Protocol behaviour at physical layer of I2C Bus
- Electrical parameter measurements must be carried out at different protocol state (example; stop bit, ack bit and so forth)
- Reference level for each of the measurement changes based on the rising or falling edge of the I2C signal transition
- Reference level is either 30% or 70% as against normally used reference level of 10% to 90% or 20% to 80%
- Validation is time consuming

Overall, measuring I2C electrical measurements demands a very high level of expertise in I2C phy layer behaviour, protocol layer, signal acquisition in oscilloscope and I2C Electrical measurement procedures. Due to complexity in I2C Electrical measurements, the results can be prone to errors.

Simplifying I2C Electrical Measurements using PGY-I2C Electrical validation and Protocol Decode Software:

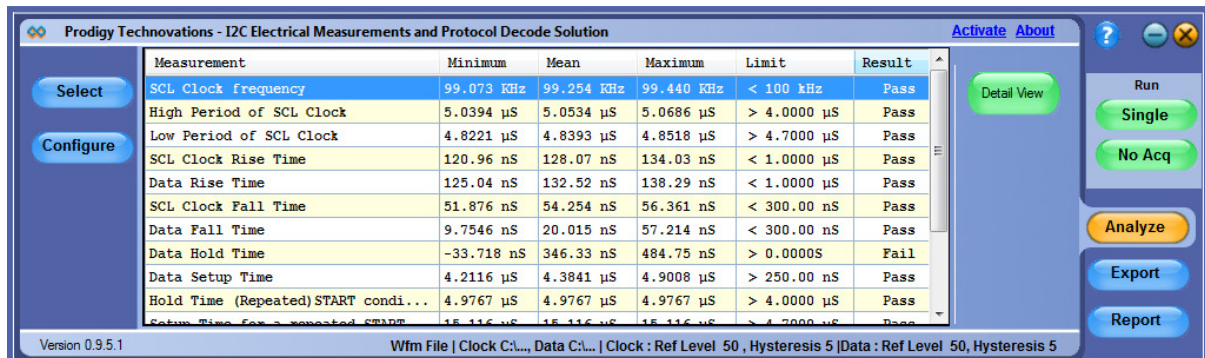
The PGY-I2C Electrical Validation and Protocol Decode Software offers electrical measurements and protocol decoding as specified in Rev 03, June 2007 I2C Bus specification. Now design and test engineers can automatically make accurate and reliable electrical measurements and decode protocols in PGY-I2C software using data acquired by Tektronix DPO5000, DPO7000, DPO/DSA/MSO70000 series oscilloscope to reduce the development and test cycle.

PGY-I2C Software runs inside Tektronix oscilloscopes. During the run operation of the application, PGY-I2C sends commands to acquire SCL and SDA signals of I2C bus. For accurate measurements, the recommended oscilloscope setup is:

- Signal is atleast 5 to 6 six main vertical divisions in the oscilloscope display with the appropriate volts per division
- Select the appropriate volts per division to display the signal with at least 5 or 6 main vertical divisions

- Select sample rate such that atleast 8 to 10 samples present in the rising or falling edge of SCL and SDA signals
- Set record length such that atleast two I2C frames are captured to make most of I2C signals.

The PGY-I2C software analyzes the acquired data for I2C protocol. The selected measurements are displayed as follows:



Measurement	Minimum	Mean	Maximum	Limit	Result
SCL Clock frequency	99.073 KHz	99.254 KHz	99.440 KHz	< 100 KHz	Pass
High Period of SCL Clock	5.0394 µs	5.0534 µs	5.0686 µs	> 4.0000 µs	Pass
Low Period of SCL Clock	4.8221 µs	4.8393 µs	4.8518 µs	> 4.7000 µs	Pass
SCL Clock Rise Time	120.96 nS	128.07 nS	134.03 nS	< 1.0000 µs	Pass
Data Rise Time	125.04 nS	132.52 nS	138.29 nS	< 1.0000 µs	Pass
SCL Clock Fall Time	51.876 nS	54.254 nS	56.361 nS	< 300.00 nS	Pass
Data Fall Time	9.7546 nS	20.015 nS	57.214 nS	< 300.00 nS	Pass
Data Hold Time	-33.718 nS	346.33 nS	484.75 nS	> 0.0000S	Fail
Data Setup Time	4.2116 µs	4.3841 µs	4.9008 µs	> 250.00 nS	Pass
Hold Time (Repeated) START condi...	4.9767 µs	4.9767 µs	4.9767 µs	> 4.0000 µs	Pass
Setup Time for a repeated START	15.116 µs	15.116 µs	15.116 µs	> 4.7000 µs	Pass

Electrical Measurement results with limits as specified in I2C standard document

The application makes each of the I2C electrical measurements in every possible I2C protocol state and displays the min, max and mean values. If mean value is within the limit specified, application shows 'Pass'. But in case, if the mean value is pass but either the min or max values exceed the limits, applications shows 'pass*' with asterisk.

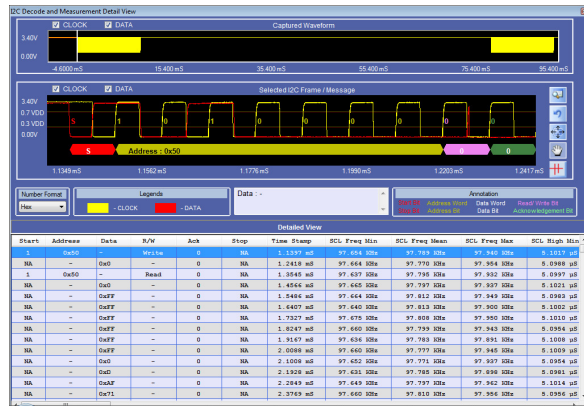
PGY-I2C makes all these measurements in an instant of time addressing all the challenges of I2C electrical measurements, giving accurate and reliable measurements.

The 'Detail View' in the Analyze pane offers protocol information and measurement for each I2C Packet. This would help in debugging I2C bus in a system. In a master-slave I2C bus, different IC s would communicate. There is possibility of interoperability issues between IC s using I2C Bus. This problem could be due following reasons.

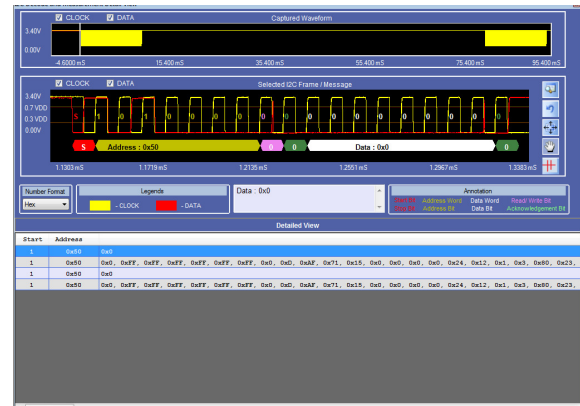
- Problems due to signal integrity in PCB
- EMI/EMC issues
- Not strict compliance to electrical characterstics of I2C Standard specification

The 'Detail view' would help in isolating interoperability issues by providing physical layer waveform, electrical measurements for each I2C message/frame and protocol decode.

The Detail view display for I2C message and I2C packet/frame is as follows.



Detail view of each I2C message

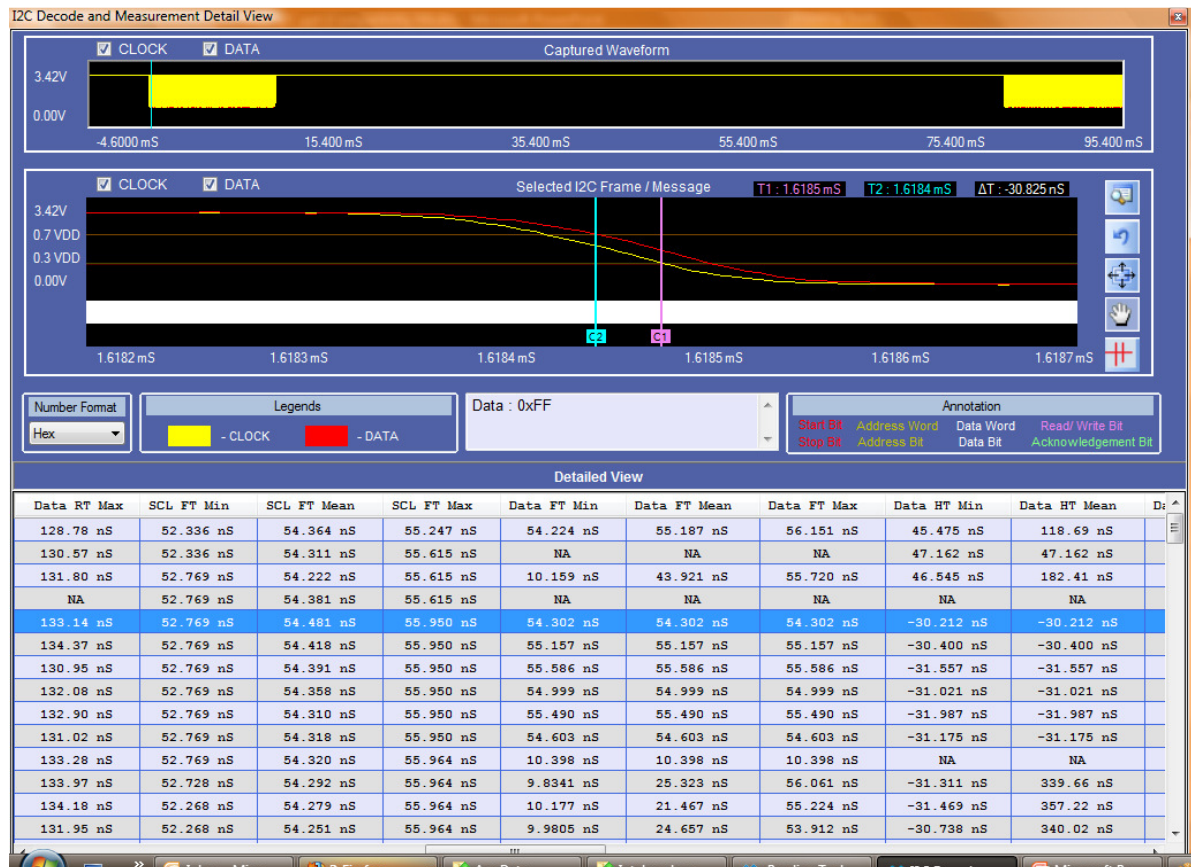


Detail view of each of I2c packet/frame

Detail view contains following information:

- Waveform plot of the acquired data
- Protocol Decode in I2C packet/frame or I2C message format
- Electrical measurements for each I2C message or I2C packet/frame
- Selected I2C message or packet/frame waveform plot with protocol decoded data overlapped on the waveform
- Utility features such as cursors, cursor time readout, zoom, undo, fit to screen and pan

Using 'Detail View' you can now debug the I2C bus for physical layer and protocol layer.



In this figure, observe that data hold time for certain I2C message has failed (refer the selected row in the result table). When you select the failed measurement in result table, the I2C waveform related to this row will be displayed on waveform window with overlapped decoded data. You can zoom into the necessary I2C signal transition edge using zoom feature and make timing measurements using cursors.

Summary:

PGY-I2C Electrical Validation and Protocol Decode software offers the industry's best I2C Electrical validation and protocol decode software. This software allows design and test engineers to characterize the I2C bus for compliance to I2C bus standard specifications.

PGY-I2C software has leading features 'Detail View' to debug I2C bus at physical layer and at protocol layer for electronic system level development.

PGY-I2C software runs inside industry leading Tektronix oscilloscopes such as DPO5000, DPO7000, DPO/MSO/DSA70000 to offer to most accurate and reliable solution.

About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and PHY layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and PHY Layer testing solutions that span the serial data, telecommunications, automotive, and defence electronics sectors worldwide.

Contacts:

Prodigy Technovations Pvt. Ltd.; 4123, 6th Cross, 19th Main, HAL II Stage, Indiranagar, Bangalore, India 560008 ; www.prodigytechno.com

Phone number: +91 80 32553020; Email: contact@prodigytechno.com

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- MIPI-MPHY-UniPRO Protocol Decode Software
- MIPI-MPHY-LLI Protocol Decode Software
- SPI Electrical validation and Protocol Analysis Software
- UART/RS232 Protocol Decode Solution
- FlexRay Protocol and SI Analysis Software
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- USB2.0 Protocol Decode Software