



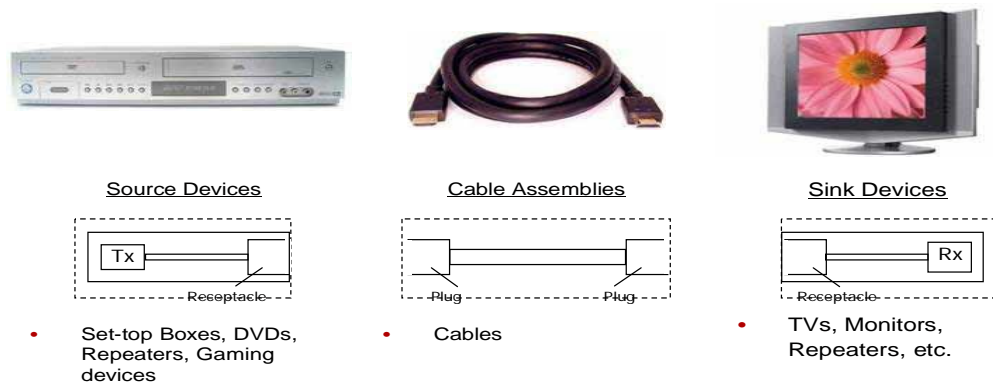
## HDMI/MHL Protocol Testing Using HDMI/MHL Protocol Analyzer

### Introduction

HDMI is a digital replacement for existing analog video standards. It is termed as the catalyst for the DTV revolution. The DTV revolution is driving the HDMI standard to support increase in data speed to higher video resolutions to meet emerging needs. As a result, design and validation engineers need tools to improve efficiency by performing a wide range of standards-required tests quickly and reliably.

This application note describes HDMI/MHL Protocol Analyzer that addresses protocol testing and validation needs as HDMI1.4a. This application uses a superior method to analyze HDMI and MHL protocol by correlating protocol data with electrical waveform for easy debug.

## HDMI /MHL protocol overview



**Fig 1 Source, Cable and Sink devices**

**HDMI:** High Definition Multimedia Interface, a compact uncompressed digital video and audio interface. HDMI system architecture is defined to consist of sources and sinks. A given device may have one or more HDMI inputs and one or more HDMI outputs. Each HDMI input on these devices has to follow all of the rules for an HDMI sink and each HDMI output shall follow all of the rules for an HDMI source.

HDMI cable and connectors carry four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio and auxiliary data. In addition, HDMI carries a VESA DDC channel. The DDC is used for configuration and status exchange between a single source and a single sink. The optional CEC protocol provides high-level control functions between all of the various audiovisual products in a user's environment.

**MHL:** The mobile high-definition link is an interface for transmitting digital television audiovisual signals from mobile phones, mobile video players, video cameras, still image cameras and other audiovisual sources to television sets, projectors, monitors and other video displays. The MHL interface is a low-pin-count high definition (HD) video interface based on the same transition minimized differential signaling (TMDS) technology used in the digital video interface (DVI).

MHL can carry high quality multi-channel audio data and can carry all standard and High-definition consumer electronics video formats. Content protection technology is available.

MHL also carries control and status information in both directions. In addition, MHL has a dedicated pin to supply power from one MHL system to another.

**Protocol Overview:** The HDMI link operates in one of three modes: Video Data Period, Data Island period, and Control period. During the Video Data Period, the active pixels of an active video line are transmitted. During the data island period, audio and auxiliary data are transmitted using a series of packets. The control period is used when no video, audio, or auxiliary data needs to be transmitted.

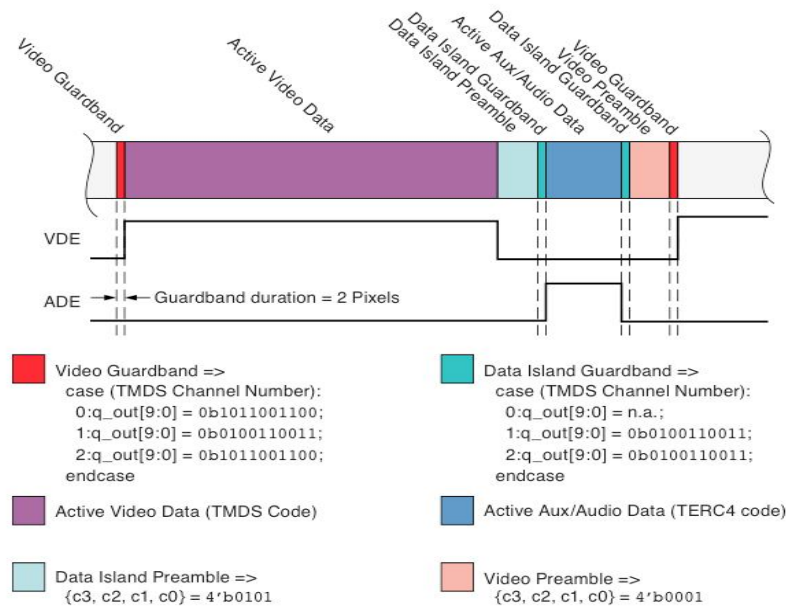


**Fig 2 Video and Audio data pictorial representation**

MODE	DATA Transmitted	Input bits/Channel	Encoding Type	Encoded Output bit/Channel/Cycle
Video Data Period (1Pixel =3bytes=24bits)	Video Pixels	8bits	Video Data Encoding (TMDS Encoding)	10bit
	Leading Guard Band (has 2 Spl Characters)	10bits	None	10bit
DATA Island Period (Min 1 Packet ,Max 18 Packets) , 1 Packet =36 Bytes	Auxillary Data Packets	4bits	TERC4 Encoding	10bit
	Audio Packets	4bits	TERC4 Encoding	10bit
	Leading Guard Band	10bits	Encoding Required only for Channel 0	10bit
	Trailing Guard Band	same as Leading Guard Band	Same as Leading Guard Band	Same as Leading Guard Band
Control Period	HSYNC/VSNC Preamble	2bits	Transition Maximized Encoding	10bit

**Table 1 HDMI/MHL data Modes**

**Video Data Period:** Video data periods are used to carry the pixels of an active video line. Each video data period is preceded by a preamble. Following the preamble, the video data period begins with a two-character video leading guard band. There is no trailing guard band for the video data period. In active video periods, 24 bits of pixel data are encoded using TMDS transition minimized encoding during each TMDS clock period.



**Fig 3 Video and Audio Data representation**

**Data Island Period:** During the data island period, audio and auxiliary data are transmitted using a series of packets. This auxiliary data includes info frames and other data describing the active audio or video stream or describing the source. Each data island is preceded by a preamble. Following the preamble, each Island starts with a leading guard band. The first packet of the data island then follows. During every TMDS clock period of the data island, including the guard band, bits 0 and 1 of TMDS channel 0 transmit an encoded form of HSYNC and VSYNC. Bit 2 of TMDS channel 0 is used to transmit the packet header. All four bits of TMDS channels 1 and 2 are used for the packet data. Each packet is 32 pixels long and is protected by BCH ECC for error detection and correction.

During the data island, each of the three TMDS channels transmits a series of 10-bit characters encoded from a 4-bit input word, using TMDS Error Reduction Coding (TERC4). TERC4 significantly reduces the error rate on the link by choosing only 10-bit codes with high inherent error avoidance.

TMDS Data Channel	8 Bit Data Lines	Control Period		Data Island Period				Control Period		Video data Period	Control Period				
		Min 4Clk	Max 8Clk	2Clk	Max 32Clk	Max 32Clk	2Clk	Min 4Clk	Max 8Clk		Min 4Clk	Max 8Clk			
Logical Channel 0	HS/Bit0	HSYNC		HSYNC				HSYNC		Leading Guard Band	Video Data	HSYNC			
	VS/Bit1	VSYNC		VSYNC				VSYNC				VSYNC			
	Bit2			1	Packet 1 Header		Packet 2 Header		1						
	Bit3			1	0	1	1		1						
	Bit4														
	Bit5														
	Bit6														
	Bit7														
Logical Channel 1	Bit0	Control Data	Preamble	Leading Guard Band	4bits of Packet1 Data Plus BCH , ECC Parity Bits		4bits of Packet1 Data Plus BCH , ECC Parity Bits		Leading Guard Band	Control Data	Preamble	Leading Guard Band	Video Data	Control Data	Preamble
	Bit1														
	Bit2														
	Bit3														
	Bit4														
	Bit5														
	Bit6														
	Bit7														
Logical Channel 2	Bit0	Control Data	Preamble	Leading Guard Band	4bits of Packet1 Data Plus BCH , ECC Parity Bits		4bits of Packet1 Data Plus BCH , ECC Parity Bits		Leading Guard Band	Control Data	Preamble	Leading Guard Band	Video Data	Control Data	Preamble
	Bit1														
	Bit2														
	Bit3														
	Bit4														
	Bit5														
	Bit6														
	Bit7														
TRANSITION MINIMIZED FROM FIXED VALUE				TRANSITION MAXIMIZED				TERC4 ENCODED				TRANSITION MINIMIZED FROM 8Bit VIDEO DATA			

Fig 4 Video/Audio data on TMDS Data Channel

**Control Period:** The Control period is used when no video, audio, or auxiliary data needs to be transmitted. Control period is required between any two periods that are not control periods.

Control period is used for transmission of the preamble. The sink for character synchronization also uses the control period.

During control periods, 2 bits per channel, or 6 bits total are encoded per TMDS clock using a transition maximized encoding. These 6 bits are HSYNC, VSYNC, CTL0, CTL1, CTL2 and CTL3. Near the end of every control period, a preamble, using the CTLx bits, indicates whether the next data period is a video data period or a data island period.

**Preamble:** Immediately preceding each video data period or data island period is the preamble. This is a sequence of eight identical control characters that indicate whether the upcoming data period is a video data period or is a data island. The values of CTL0, CTL1, CTL2, and CTL3 indicate the type of data period that follows. The remaining control signals, HSYNC and VSYNC, may vary during this sequence.

CTL0	CTL1	CTL2	CTL3	Data Period Type
1	0	0	0	Video Data Period
1	0	1	0	Data Island Period

Table 2 Data Period Type

## Challenges in Validating HDMI/MHL Interface

An HDMI technology provider needs to comply with the HDMI/MHL specification provided by the HDMI/MHL consortium. The HDMI/MHL protocol analysis software embeds the HDMI1.4a and MHL 2.0 Compliance Test procedure, ensuring dependable results.. There are number of tests to be carried out at

the protocol layer. This test requires complex measurement techniques using dedicated HDMI/MHL protocol analyzers. These instruments offer engineers visibility into the logic state of the signal without correlation to the clock and data. Many times, protocol irregularities are hidden in the electrical signals in Phy layer and logical layer.

Some of the drawbacks and challenges faced by the engineers during validation are listed below:

- Lack of a single tool or instrument to handle physical and Protocol layer challenges
- Difficulty in correlating the data from Protocol with Physical layer
- Increasing complexity of the test system due to multiple equipments.
- There are no instruments that provide overhead information along with payload (actual image)
- No seamless synchronization possible from mapping the failure of a protocol test to actual electrical signal and location in the HDMI frame (overhead and payload)

## List of HDMI/MHL Compliance Tests

### Source Protocol [HDMI/MHL]

- Legal Codes
- Basic Protocol
- Extended Control Period
- Packet Types

### Source Video [HDMI/MHL]

- Pixel Encoding
- Video Format Timing
- Pixel Repetition
- AVI Info Frame

### Source Audio [HDMI/MHL]

- IEC 60958/IEC 61937
- ACR
- Audio Sample Packet Jitter
- Audio Info Frame
- Audio Sample Packet Layout

### Source Interoperability with DVI

- Interoperability with DVI

### Source Advanced Features

- Deep Color
- Gamut Metadata Transmission
- High Bitrate Audio
- One Bit Audio
- 3D Video Format Timing
- 4K x 2K Video Format Timing\* - Limited support
- Extended Colorimetry Transmission

**Source Protocol:** In this phase of testing, various modes and features supported by the source are tested. The HDMI source needs to go through this test to adhere to the HDMI protocol.

**Legal Codes:** Verify that Source only outputs legal 10-bit codes. Verify that, for all pixels within the analysis period, the Source DUT transmits only 10-bit values on each of the three TMDS channels that correspond to one of the following:

- Legal Video Data codes
- 4 Control Period codes
- 16 TERC4 codes
- Data Island Guard Band (all 4 possible values for Channel 0)
- Video Guard Band



**Basic Protocol:** The objective of basic protocol test is to verify that the HDMI source transmits valid code sequences. The valid code sequence consists of control periods, data island periods and video data periods. This test verifies the following overhead information:

- Data Island and Video Data periods are preceded by the preamble.
- Sequence of preamble is intact indicating that the upcoming data period is a Video Period or is a Data Island.
- Source transmits code sequences for Control Periods, Data Island Periods and Video Data Periods corresponding to basic HDMI protocol rules.

**Extended Control Period:** The objective of the extended control period test is to verify that HDMI source transmits a valid extended control period within the required period specified for each frame format. This test verifies the following HDMI overhead information.

Source transmits an extended control period. This should be transmitted periodically with the minimum periodicity of 32Tpixels or maximum of 50msec.

**Packet Types:** The objective of the packet type test is to verify that HDMI source transmits permitted packet types during data island period. This test verifies following HDMI overhead information:

- Null Packet Type
- ACR Packet Type
- Audio Sample Packet Type
- General Control Packet Type
- Source Video

**Source Video:** The objective of source video test is to verify HDMI source DUT connector type i.e. TYPE A or TYPE B. This test verifies following HDMI overhead information:

- Type A transmits video format timing supported by EDID
- Type B transmits any video format timing

**Pixel Encoding:** The objective of the pixel-encoding test is to verify that the HDMI source DUT always transmits data using required pixel encoding scheme. This test verifies following HDMI overhead information.

- HDMI sources support either YCbCr 4:2:2 or YCbCr 4:4:4 pixel
- AVI infoframe is transmitted on every video field.
- Examine video output and all AVI infoframe transmitted from Source.

**Video Formatting Timing:** The objective of the video formatting timing test is to verify HDMI Source DUT transmits any video format timing defined as per the EIA/CEA-861B. This test verifies following HDMI overhead information.

- Complies with all required pixel and line counts and pixel clock frequency range
- Video line pixel counts and video field line counts (both active and total) and HSYNC and VSYNC positions.
- Pixel clock is within or outside of allowable range.
- VSYNC or HSYNC relationship for two video fields.

**Pixel Repetition:** The objective of the pixel repetition test is to verify that the pixel is repeated for the numbers of time specified in the AVI. This test verifies following HDMI overhead information.

- Valid Pixel Repeat Values for Each Format

**AVI InfoFrame:** The objective of AVI infoframe test is to verify that accurate AVI InfoFrame is transmitted on every video field when required. This test verifies following HDMI overhead information.

- Determines that the source and sink support the AVI InfoFrame.
- Verify source will send this information to the DTV monitor once per frame.
- AVI InfoFrame needs to be transmitted once per field whenever source supports the transmission of the AVI InfoFrame.
- AVI shall be sent when Source is transmitting any video format timing listed in EDID with multiple aspect ratios.
- AVI InfoFrame shall be transmitted whenever the HDMI source uses alternate colorimetry.
- Transmitting a non-861B-defined format, any transmitted AVI InfoFrame, VIC field needs to be zero
- The information like Active Format Aspect Ratio, bar widths, over/under scan, non-uniform picture scaling and etc.,
- The information that can be made used by the sink device, if the valid information is present at the source device.

**Source Audio:** Tests will be performed at each of the following three combinations of video and audio formats. One of the Source-supported mandatory video formats (480p, 576p or 640x480p) and an audio format with the highest Audio Sample packet rate is available.

**IEC 60958/IEC 61937:** The objective of IEC 60958/IEC 61937 test is to verify that the audio sample carried during data island period follows the rules defined by the IEC 60958 or IEC61937.

Layout Value	Max Num Channels	Samples	Subpkt0	Subpkt1	Subpkt2	Subpkt3
0	2	4	Chnl 1,2 Sample 0	Chnl 1,2 Sample 1	Chnl 1,2 Sample 2	Chnl 1,2 Sample 3
1	8	1	Chnl 1,2 Sample 0	Chnl 3,4 Sample 0	Chnl 5,6 Sample 0	Chnl 7,8 Sample 0

**Table 3 Audio sample**

This test checks for the number of samples present within the Audio Sample Subpackets. Layout 0 can carry up to 4 samples from a single IEC 61937 or from a single 2-channel IEC 60958 stream of audio. Layout 1 can be used to carry one audio sample with three to eight channels of L-PCM audio.

**ACR:** The objective of ACR test is to verify that the relationship between the parameters (N, CTS, audio sample rate) is correct with respect to the Audio Clock Regeneration mechanism. This test verifies following HDMI overhead information:

- Count the number of audio samples (n) over 2 seconds (Ts)
- N parameter value.
- CTS parameter value

**Audio Sample Packet Jitter:** The objective of audio sample packet jitter is to verify that the source audio packets jitter is within the limits specified.

**Audio InfoFrame:** The objective of audio infoframe is to verify that source transmits an audio InfoFrame whenever required and that contents are valid. This test verifies the following HDMI overhead information:

- Check Audio InfoFrame placement
- Examine the placement of the Audio InfoFrame Packet
- Check Packet Header
- Check Packet Body
- Check for illegal CA
- Digital audio supported by the sink.
- Source transmits an Audio InfoFrame whenever required and that contents are valid.



**Audio Sample Packet Layout:** The objective of audio sample packet layout test is to verify the Layout type used by the source to transmit the audio information is valid. This test verifies following HDMI overhead information

- Source and sink devices support audio format more than basic audio, then this information is sent using the audio identification information to the sink.

**Source Interoperability with DVI:** The objective of source interoperability is to verify that all HDMI sources or sinks shall be compatible with DVI 1.0 compliant source and sink devices (i.e. "monitors" or "displays", "systems" or "host ") through the use of a passive cable converter.

**Interoperability with DVI:** The Objective of interoperability with DVI test is to verify that Source never outputs a Video Guard Band or Data Island to a device without an HDMI VSDB.

- Video pixel encoding shall be RGB.
- No Video Guard Bands shall be used.
- No Data Islands shall be transmitted.

## Source Advanced Features

**Deep Color:** In deep color mode, source and sink each capture the packing phase and color depth of the last pixel character of a Video Data Period. Source communicates with general control packet (GCP) occasionally to communicate the current color depth and the packing phase of the last pixel character sent prior to the GCP. The GCP data is valid whenever CD (CD0, CD1, CD2, CD3) is non- zero.

Sink compares its own color depth and phase with the CD data, whenever the Sink receives a GCP with non-zero CD data. If they do not match, the Sink should adjust its color depth and/or phase to match the CD data. Once a Source sends a GCP with non-zero CD to a sink, it should continue sending GCPs with non-zero CD at least once per video field even if reverting to 24-bit color, as long as the Sink continues to support Deep Color.

If the Sink does not receive a GCP with non-zero CD for more than 4 consecutive video fields, it should exit deep color mode (revert to 24-bit color).

### Color Depth (CD Field) Values

CD3	CD2	CD1	CD0	Color Depth
0	0	0	0	Color Depth not indicated
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	24 bits per pixel
0	1	0	1	30 bits per pixel
0	1	1	0	36 bits per pixel
0	1	1	1	48 bits per pixel
All Other Values				Reserved

**Table 4 Color Depths**

## Pixel Packing Phase (PP Field) Values

PP3	PP2	PP1	PP0	Pixel Packing Phase
0	0	0	0	Phase 4 (10P4)
0	0	0	1	Phase 1 (10P1, 12P1, 16P1)
0	0	1	0	Phase 2 (10P2, 12P2)
0	0	1	1	Phase 3 (10P3)
0	1	0	0	Reserved
All Other Values				Reserved

Table 5 Pixel Packing Phase

## HDMI/MHL Validation Test Setup

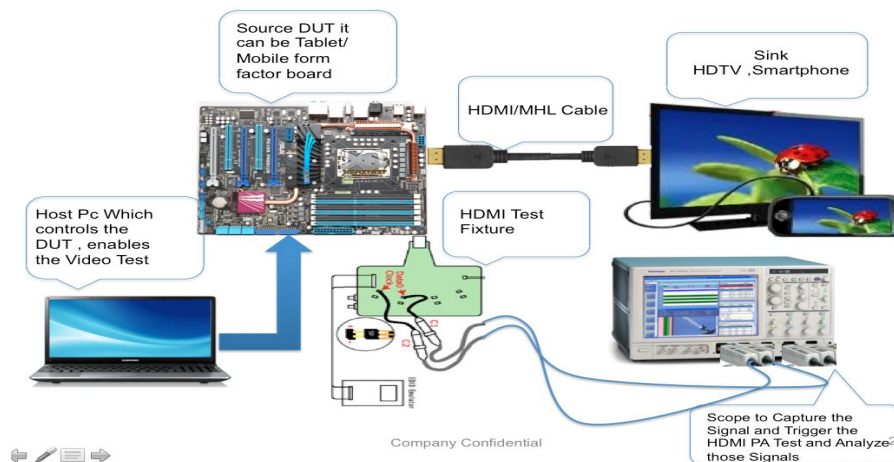


Fig 5 HDMI Validation Setup

A HDMI Test setup consists of DUT (Tablet/Smartphone) which is configured by the host to execute the video content at different resolutions on the HDTV via HDMI/MHL interface. The HDMI test fixture captures and displays the HDMI/MHL signal onto the oscilloscope. HDMI SW carries out the protocol test on this HDMI/MHL signal displayed on the oscilloscope.

## HDMI/MHL Protocol Analysis Software

The industry's first oscilloscope-based TEK-PGY-HDMI/MHL Protocol Analysis software analyzes every event in the HDMI stream from HDMI/MHL frame including phy layer which conventional protocol analyzers cannot accomplish.

TEK-PGY-HDMI/MHL Protocol Analyzer software performs the HDMI/MHL protocol compliance tests as per MHL CTS 2.0 and HDMI CTS 1.4a standards. It provides unmatched flexibility in analyzing, debugging, and correlating the test results from HDMI/MHL Frame to physical layer analog waveforms.

## Performing the tests using the TEK-PGY HDMI/MHL

Tek-PGY-HDMI/MHL Software allows the engineer to select protocol test and analysis views of the results. The Configuration panel allows the engineer to configure the HDMI/MHL video format so that application analyzes signal for set video format. One of the difficult tasks is to capture HDMI/MHL signals in an oscilloscope. The HDMI/MHL Software simplifies this task by automatically setting the volts per division, times per division and record length. To capture the complete video frame, the oscilloscope needs to be equipped with minimum of 250MB record length so that one full video frame is captured. Audio jitter tests need 20 video frames to be analyzed for audio test. This test has been implemented using parallel processing of acquisition and analysis of acquired signals using multithread implementation in HDMI/MHL Software. When 20 video frames are selected during capture in HDMI/MHL software, the application drives the oscilloscope to acquire HDMI/MHL signals and another thread analyses for protocol tests while oscilloscope is capturing next HDMI/MHL frame.

TEK-PGY HDMI/MHL protocol result panel shows all measurement results with their spec limits, pass/fail results.

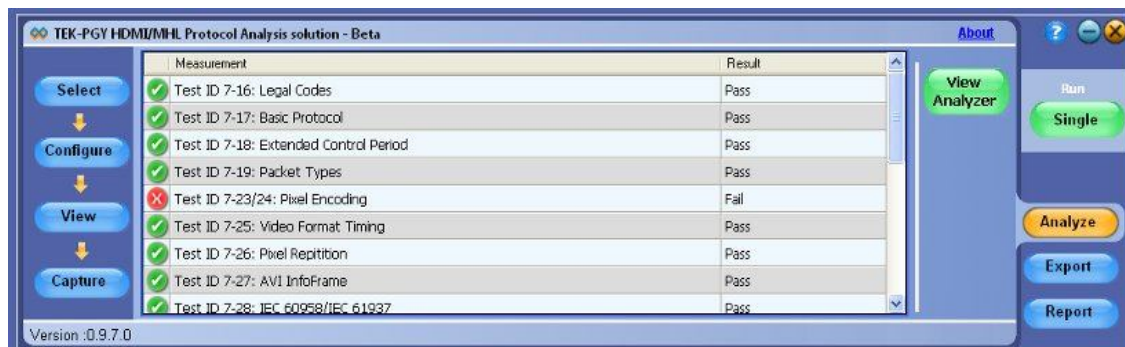


Fig 5 Analyse Window

This has Protocol test report as per HDMI1.4a and MHL 2.0 CTS.

However, when test fails there is a need analyze the cause for failure. HDMI/MHL Software provides multiple views of captured in data in different view formats. The view formats are

- Event Viewer
- Frame Viewer
- Bus Viewer
- Data packet Viewer
- Protocol viewer

Event viewer lists all the details for a test to be pass or fail. By selecting any test, you can view the test description and reason for pass or fail. Event Viewer displays the event activity to any measurement of interest. If the engineer comes across any failed test on the analyzer window, then the engineer can navigate through the event viewer and summarize each activity on each failed or passed test.

Event Viewer		
Test Name	Result	
Test ID 7-16: Legal Codes	Pass	
Test ID 7-17: Basic Protocol	Pass	
Test ID 7-18: Extended Control Period	Pass	
Test ID 7-19: Packet Types	Pass	
Test ID 7-23/24: Pixel Encoding	Pass	
Test ID 7-25: Video Format Timing	Fail	
Pixel	Test	Event Description
0	Test ID 7-16: Legal Codes	(7-16) All pixels should consist of encoding combination of three channels
539997	Test ID 7-16: Legal Codes	No error -> TEST PASS!
0	Test ID 7-17: Basic Protocol	(7-17) Basic Protocol The Packet Type should be valid
539997	Test ID 7-17: Basic Protocol	No error -> TEST PASS!
0	Test ID 7-18: Extended Control Period	(7-18) Extended Control Period should be transmitted within 50msecs after the

Fig 5 Event Viewer

Different view types are available, making it simple to move back and forth between different views of the HDMI/MHL data for in-depth analysis.

- Frame summary view
  - Helps to quickly locate the frames with error for detailed analysis.
- Bus Viewer
  - Shows the Bus activity along with the H Sync and V Sync.
- Frame Viewer
  - Displays Complete frame view with image and horizontal and vertical blanking periods.
- Event Viewer
  - Shows the test status and details of test.
- Data Packet Viewer
  - Details about the Data Island period.
- Protocol Viewer
  - Lists the protocol information in tabular format.

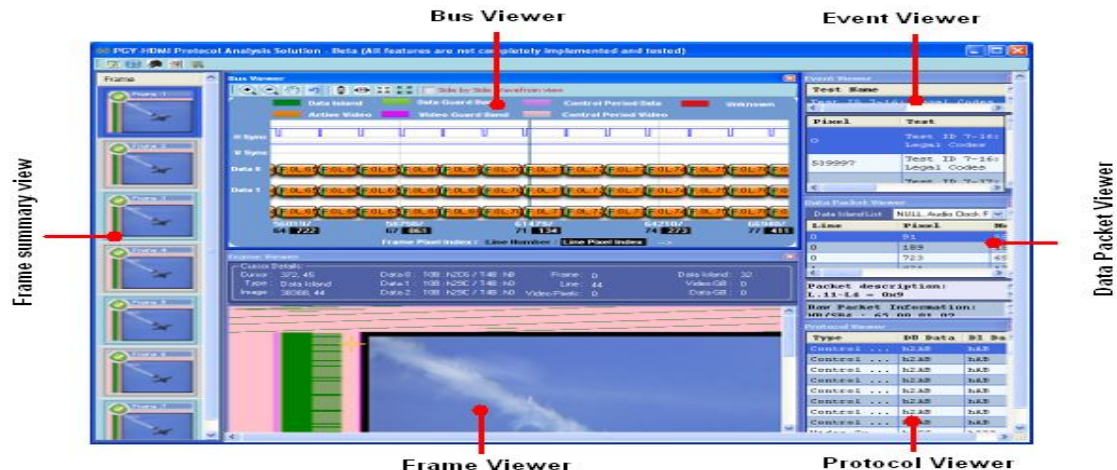


Fig 8 Different viewer options

Engineer is provided with the thumbnails for identifying image errors. HDMI SW provides quick Pass/Fail/Discard indication for error frame identification. By clicking a pixel in the frame view, the corresponding pixel in bus view and protocol view will be zoomed and highlighted for correlation.

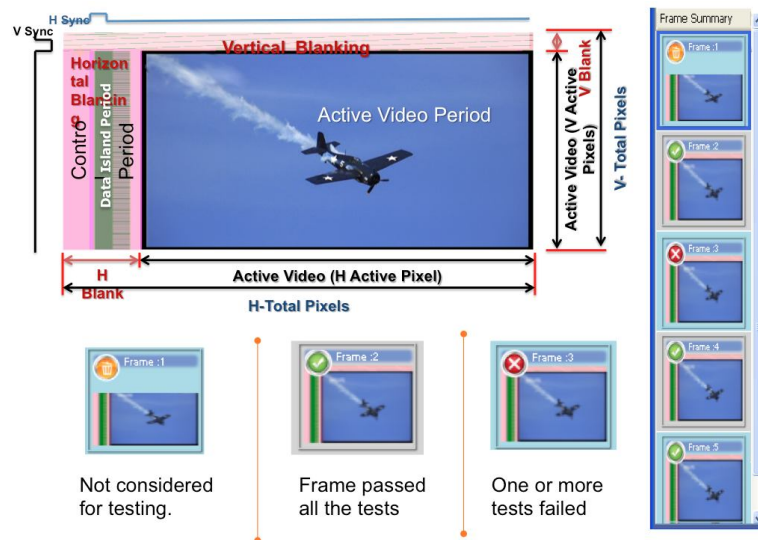


Fig 9 Frame Summary

In case a failure is seen during data island period, engineer can analysis the different types of data island packet along with the information related to the respected frame like Line number, Pixel number, and message number.

Data Packet Viewer					
Data Island List: NULL, Audio Clock Regeneration (N/CTS), Audio Sample (L-PCM and IE)					
Type	Line	Pixel	Message	BCH0	BCH1
Audio InfoF...	5	149	4340	0x7D0000...	0x000000...
AVI InfoFrame	5	149	4372	0x5B0000...	0x000000...
Source Prod...	5	149	4404	0x625049...	0xFA3233...
Vendor-Spec...	5	149	4436	0x0C0000...	0x000000...
Audio Sampl...	5	340	4627	0xCA8800...	0x000000...
Audio Sampl...	6	39	5190	0xFACCO2...	0x000000...
Audio Sampl...	6	601	5752	0xCA8803...	0x000000...
Audio Sampl...	7	300	6315	0x398004...	0x000000...

Packet description:  
 RGB or YCbCr, Y1-Y0 = 0b10 (YCbCr 4:4:4) of PB1 (0x5d)  
 YCC Quantization Range, YQ1-YQ0 = 0b00 (Limited Range) of  
 Active Format Information Present, A0 = 0b10 of PB1 (0x5d)  
 Bar Info, B1-B0 = 0b11 of PB1 (0x5d)  
 Scan Information, S1-S0 = 0b01 of PB1 (0x5d)  
 Colorimetry, C1-C0 = 0b01 of PB2 (0x68)  
 Picture Aspect Ratio, M1-M0 = 0b10 of PB2 (0x68)  
 Active Format Aspect Ratio, R3-R0 = 0b1000 of PB2 (0x68)  
 Non-uniform Picture Scaling, SC1-SC0 = 0b00 of PB2 (0x68)  
 Video Format Identification Code, VIC6-VIC0 = 18 of PB4 (0x00)  
 Pixel Repetition factor, PR3-PR0 = 0b0000 of PB5 (0x00)  
 Line Number of End of Top Bar (lower 8 bits) of PB6 = 0x0  
 Line Number of End of Top Bar (upper 8 bits) of PB7 = 0x0  
 Line Number of Start of Bottom Bar (lower 8 bits) of PB8 = 0x0

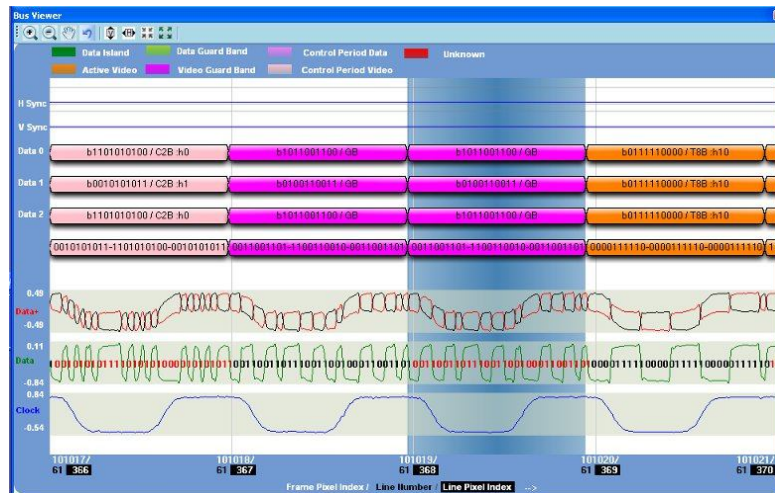
Raw Packet Information:  
 HB/SB4 (HB0-HB3 Parity): 82 02 0D E4  
 SB0 (PB00-PB06 Parity): 98 5D 68 00 12 00 00 5B  
 SB1 (PB07-PB13 Parity): 00 00 00 00 00 00 00 00  
 SB2 (PB14-PB20 Parity): 00 00 00 00 00 00 00 00  
 SB3 (PB21-PB27 Parity): 00 00 00 00 00 00 00 00

Fig 10 Data Packet Viewer

If the engineer suspects the failure due to protocol implementation or due to data transaction on either one of the 3 TMDS channel not adhering to the protocol. Engineer can verify the failure by navigating through the protocol viewer and analyzing whether each data on the TMDS channel is adhering to the protocol.







**Fig 13 Bus Viewer**

- Displays the HDMI/MHL transmission in the bus diagram.
- Shows the multiplexed MHL data and de-multiplexed logical channels as per the specification.
- For MHL Data +Ve and Data –Ve signals, the common mode clock and data are shown.
- Utility functions such as Zoom, Un-zoom, Pan, Un-do, Fit vertical, Fit horizontal, Fit complete screen and show waveform help to navigate the bus diagram.
- The X-axis provides frame pixel index, line index, line pixel index for quick pixel identification.

## Summary

The industry's first oscilloscope-based HDMI/ MHL Protocol Analyzer provides superior debugging capabilities. HDMI/ MHL Protocol Analyzer provides in-depth visibility from HDMI/ MHL Frame to Physical Layer signals, which no other protocol analyzer can provide. Cross-linking between Frame Summary Viewer, Frame Viewer, Bus Diagram Viewer, Event Viewer, Data Island Packet Viewer provides more flexibility in debugging Physical Layer and Protocol Layer problems. It is a single box solution for debugging Physical and Protocol Layer. An oscilloscope can be used for Physical Layer and Protocol Layer Testing providing more return on your investment on your oscilloscope.

## About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd ([www.prodigytechno.com](http://www.prodigytechno.com)) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.

## Other products:

- HDMI and MHL Protocol Compliance Test Software
- MIPI UniPRO and LLI Protocol Decode Software
- MIPI UFS Protocol Decode Software
- HSI Electrical Validation and Protocol Decode Software
- I2C Electrical validation and Protocol Decode Software
- SPI Electrical Validation and Protocol Decode Software
- I2S Electrical, Audio, and Protocol Testing Software
- UART/RS232 Protocol Decode Solution
- FlexRay Protocol and SI Analysis Software
- USB2.0 Protocol Decode Software
- HSIC Protocol Decode Software