



Logic Analyser

for Embedded Interfaces analysis

The Discovery logic analyzer series, PGY-LA-EMBD has the built-in capability to debug I2C protocol, SPI protocol, UART and many other serial protocols. This is a PC based logic analyzer designed for professional engineers. The Discovery logic analyzer is used to debug embedded systems, the logic analyzer not only reduces the workbench area but also allows it to have a very small form factor and can be used to debug failures in the field. The protocol decode capabilities are designed to debug the logic and protocol issues faced by embedded design teams in consumer, industrial, home automation, health, and education sectors.

PGY-LA-EMBD is an industry first logic analyzer in its category which enables engineers to debug timing problems and perform simultaneous protocol analysis of I2C, SPI, UART or I3C, SPMI and RFFE in embedded designs. This enables designers to debug circuit level and system level problems quickly.

PGY-LA-EMBD offers 1GS/Sec Asynchronous (timing) data and 100MHz Synchronous (state) data capture which makes it an ideal debug tool to address the digital design problems. Designers can now easily analyze setup and hold time issues, glitches and synchronous data activities apart from analyzing protocol issues.

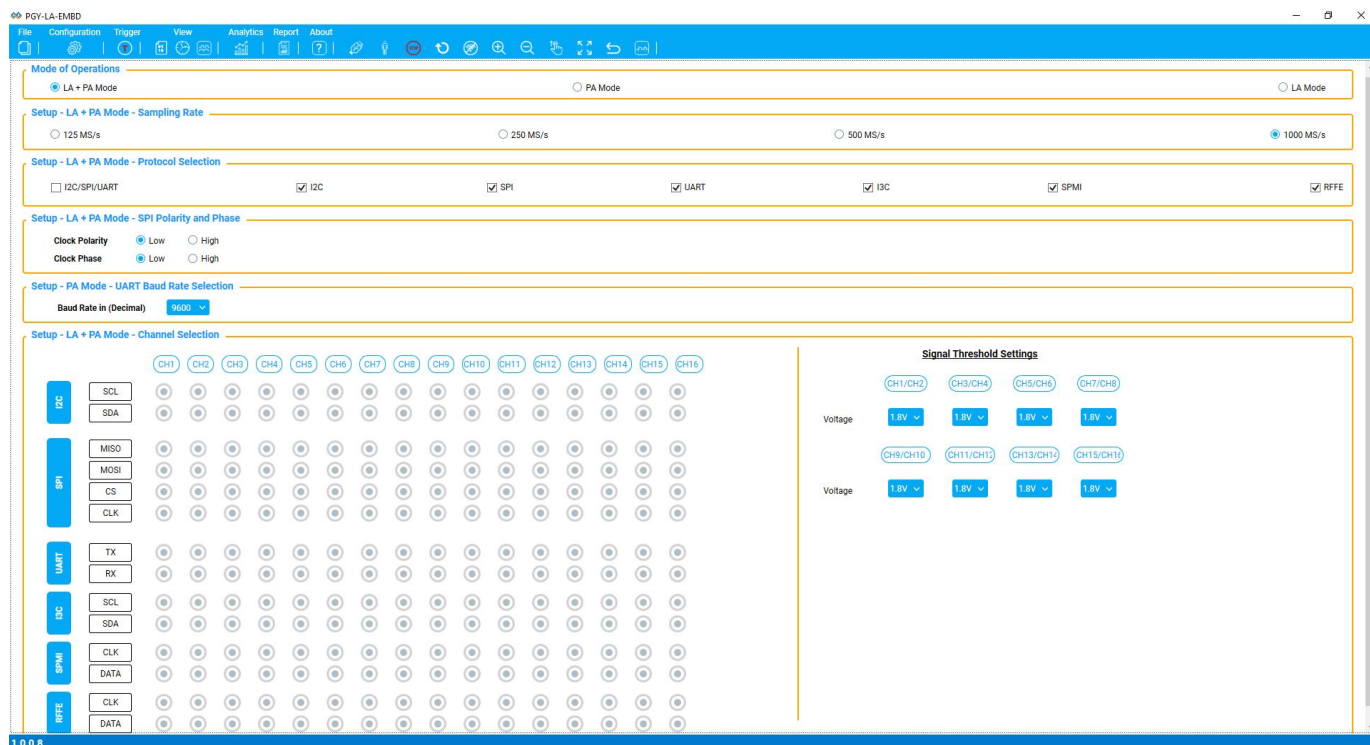
Current generation embedded designers need to collect data from multiple interfaces such as I2C, SPI, UART, I3C, SPMI, RFFE and process it to achieve optimal performance of their design. Embedded design teams need to take timely action to meet the intended objectives of the product. PGY-LA-EMBD decodes I2C, SPI, UART or I3C, SPMI, RFFE bus and displays the protocol activity with time stamp information. PGY-LA-EMBD is an ideal instrument to debug hardware and embedded software integration issues and optimize the software performance.

Multiple Markers enable smart delta measurements which are key to designers. Zoom enables users to look at specific areas of the signal.

Key Features

- ✦ 10 channels with Protocol and Logic Analysis capability.
- ✦ 1GS/Sec Timing (Asynchronous) Analysis.
- ✦ 100MHz State (Synchronous) Analysis.
- ✦ Simultaneous Protocol Analysis of I2C-SPI-UART and I3C-SPMI-RFFE.
- ✦ Detailed Trigger capabilities: Auto, Pattern, Protocol aware (I2C, SPI, UART, I3C, SPMI, RFFE) and Timing (Pulse Width and Delay Trigger).
- ✦ Smart streaming of data from Protocol Analyzer to host computer for long duration capture using USB 3.0 interface.
- ✦ Innovative easy to use Graphical user interface.
- ✦ Error Analysis of Protocol packet.
- ✦ Provides Timing, Waveform, Listing and Protocol listing views.
- ✦ Detailed filtering capability for protocol decoded data.
- ✦ PDF and CSV report format.
- ✦ API support.

Easy Configuration



PGV-LA-EMBD

File Configuration Trigger View Analytics Report About

Mode of Operations

☒ LA + PA Mode ☐ PA Mode ☐ LA Mode

Setup - LA + PA Mode - Sampling Rate

☐ 125 MS/s ☐ 250 MS/s ☐ 500 MS/s ☒ 1000 MS/s

Setup - LA + PA Mode - Protocol Selection

☐ I2C/SPI/UART ☒ I2C ☒ SPI ☒ UART ☒ I3C ☒ SPMI ☒ RFFE

Setup - LA + PA Mode - SPI Polarity and Phase

Clock Polarity ☒ Low ☐ High

Clock Phase ☒ Low ☐ High

Setup - PA Mode - UART Baud Rate Selection

Baud Rate in (Decimal)

Setup - LA + PA Mode - Channel Selection

CH1 CH2 CH3 CH4 CH5 CH6 CH7 CH8 CH9 CH10 CH11 CH12 CH13 CH14 CH15 CH16

I2C

SCL

SDA

SPI

MISO

MOSI

CS

CLK

UART

TX

RX

I3C

SCL

SDA

SPMI

CLK

DATA

RFFE

CLK

DATA

Signal Threshold Settings

CH1/CH2 CH3/CH4 CH5/CH6 CH7/CH8

Voltage

CH9/CH10 CH11/CH12 CH13/CH14 CH15/CH16

Voltage

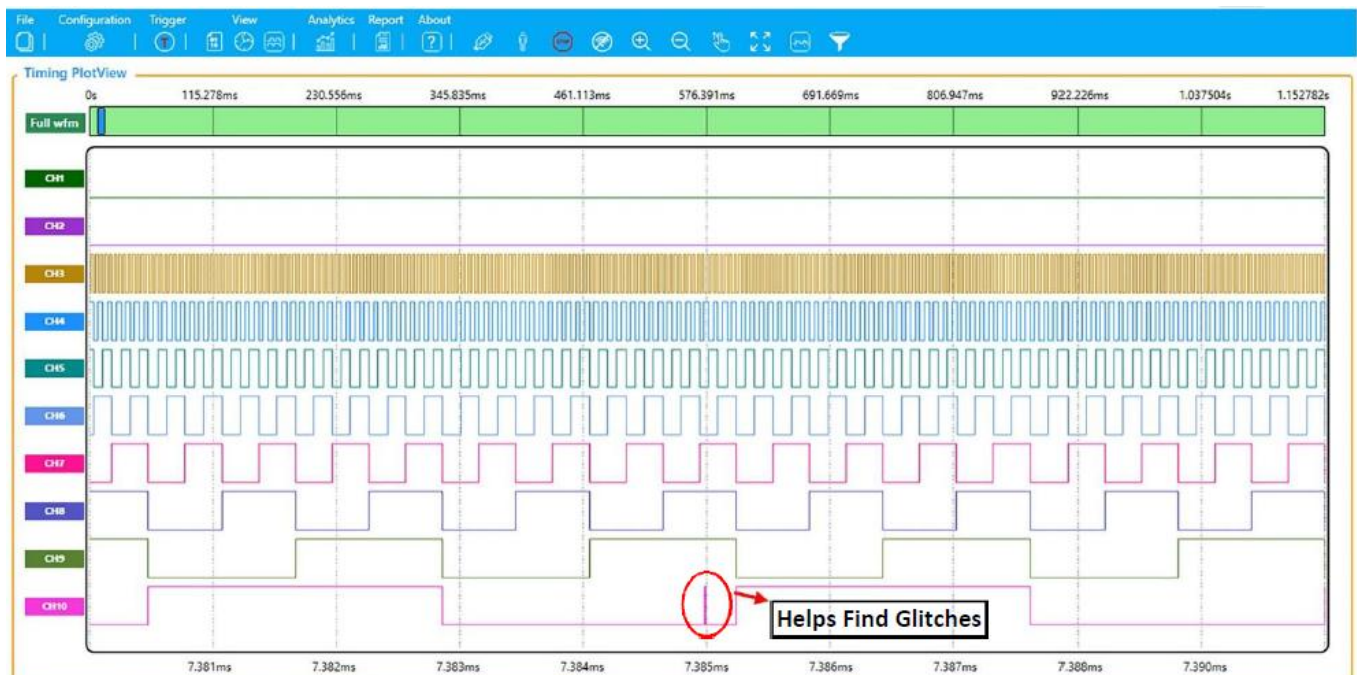
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Users can easily configure the Logic Analyzer for embedded interfaces by either selecting Logic Analysis (LA) mode or Protocol Analysis (PA) mode or a combined (LA+PA) mode. This ensures a quick and easy way to configure the product and look at complex problems at system level either in Logic Analysis (State Analysis, Timing Analysis) or Protocol decoding or both. Save and Recall capability ensures designers can recall their custom setup details.

Multiple Domain

Multiple domain Views provide the necessary complete view of all supported interface states, timing and protocol activity. Users can easily setup the analyzer to view timing, logic and decode views to enable easy insights to the design. Users can set different trigger conditions from the setup menu to capture Timing and Protocol activity at specific events. The decoded results can be viewed in Timing, Logic and Protocol listing window with auto correlation. This comprehensive view of information makes it industry's best, offering an easy to use solution to debug the embedded interfaces protocol activity and analyze timing issues. Multiple cursors help designers to look into details of their design performance.

Timing View



Timing view is a unique capability of the PGY-LA-EMBD which enables designers to get detailed insights into their signal's timing information. The timing view uses an internal clock signal to plot the waveform. The flexible sampling rate selection enables designers to investigate Glitches that can cause issues in the functioning of their designs. Grouping feature enables designers to group various related signals for better viewing and analysis. Marker and Zoom features make it convenient to analyze any timing errors.

Ability to analyze any point in the captured data record ensures easy debugging and analysis over a long capture duration.

State View/Waveform Listing View

PGY-LA-EMBD

File Configuration Trigger View Analytics Report About

Waveform Listing

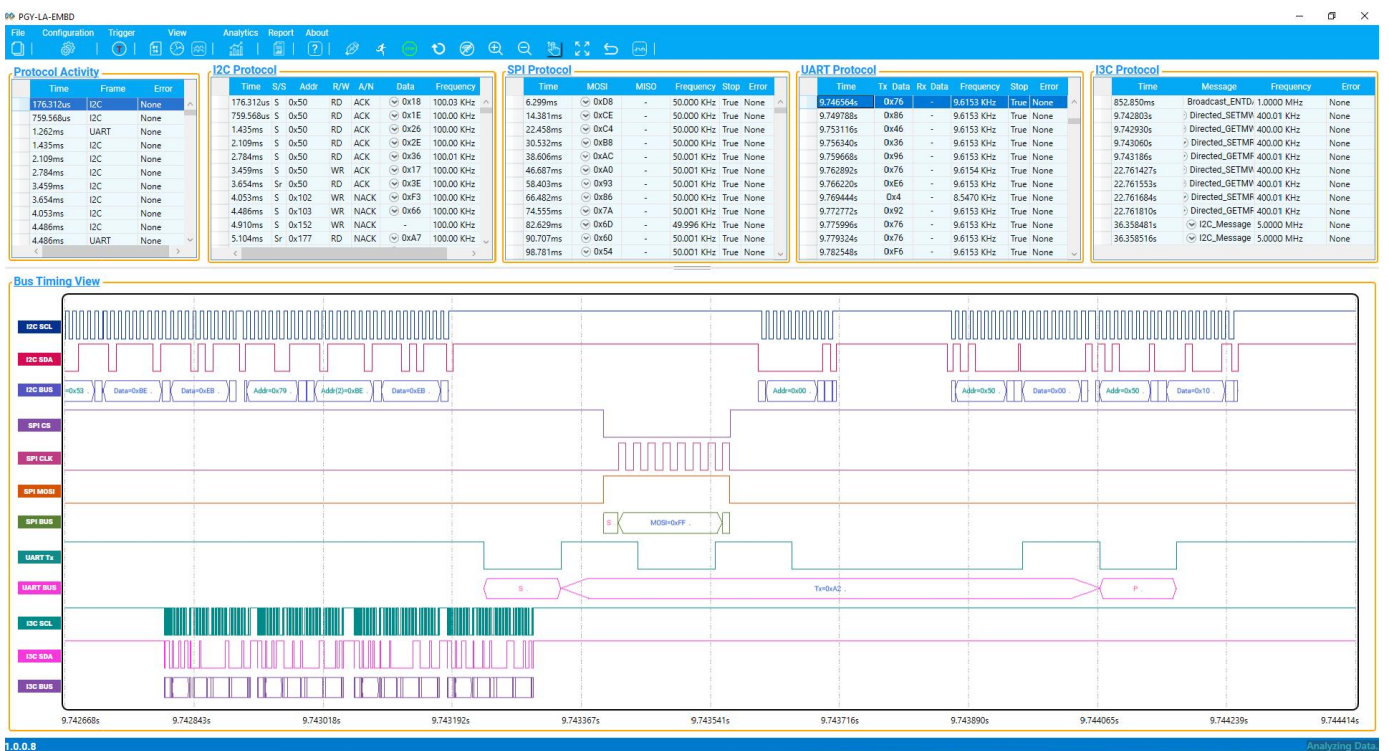
Markers M1 To M2 0s M3 To M4 0s M5 To M6 0s Data Format Hex

| Sample | Timestamp | CH16-UART TX | CH15-SPI Clk | CH14-SPI MOSI | CH13-SPI CS | CH12-I2C Data | CH11-I2C Clk | CH10-I3C Data | CH5-I3C Clk |
|--------|-----------|--------------|--------------|---------------|-------------|---------------|--------------|---------------|-------------|
| 0 | 0s | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 171.320us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 2 | 176.312us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 3 | 179.128us | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 4 | 181.608us | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 5 | 186.312us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 6 | 188.816us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 7 | 191.608us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 8 | 196.312us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 9 | 199.128us | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 10 | 201.608us | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 11 | 206.312us | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 12 | 208.816us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 13 | 211.608us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 14 | 216.312us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 15 | 221.608us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 16 | 226.312us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 17 | 231.608us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 18 | 236.312us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 19 | 241.608us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 20 | 246.320us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 21 | 249.128us | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 22 | 251.608us | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 23 | 256.320us | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 24 | 256.464us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 25 | 261.608us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 26 | 266.320us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 27 | 273.536us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 28 | 278.240us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 29 | 283.536us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 30 | 288.240us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 31 | 293.536us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 32 | 298.240us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 33 | 298.720us | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 34 | 303.536us | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 35 | 308.240us | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 36 | 313.536us | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 37 | 318.240us | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 38 | 318.400us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 39 | 323.536us | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 40 | 328.240us | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

1.0.0.8 Analyzing Data

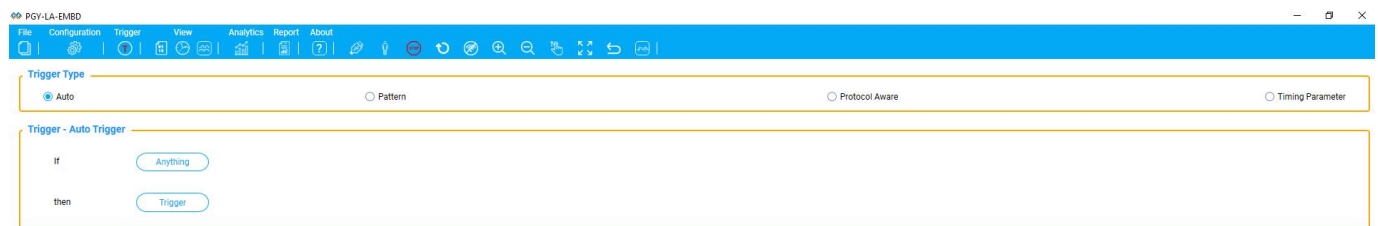
State view helps designers to see the actual signal behavior. Using the device clock as reference, it provides the plot of clock and data signals with bus diagram. Grouping of signals ensures designers have the flexibility to view signals together. All signals are time correlated to help look into setup and hold times, pulse width, missing data, etc. which are very critical for digital designs as designers look to optimize their codes.

Protocol Decode View



Protocol Activity window provides the decoded packet information in each state and all packet details with error info in the packets. This gives the system level insight to the design teams. The individual protocol decodes windows based on selected interfaces ensuring easy view ability for design teams. The Selected frame in Protocol listing window will be auto correlated in timing view to view the timing information of the packet. Protocol errors will be highlighted to ensure designers are alerted to the same easily.

Powerful Trigger Capabilities



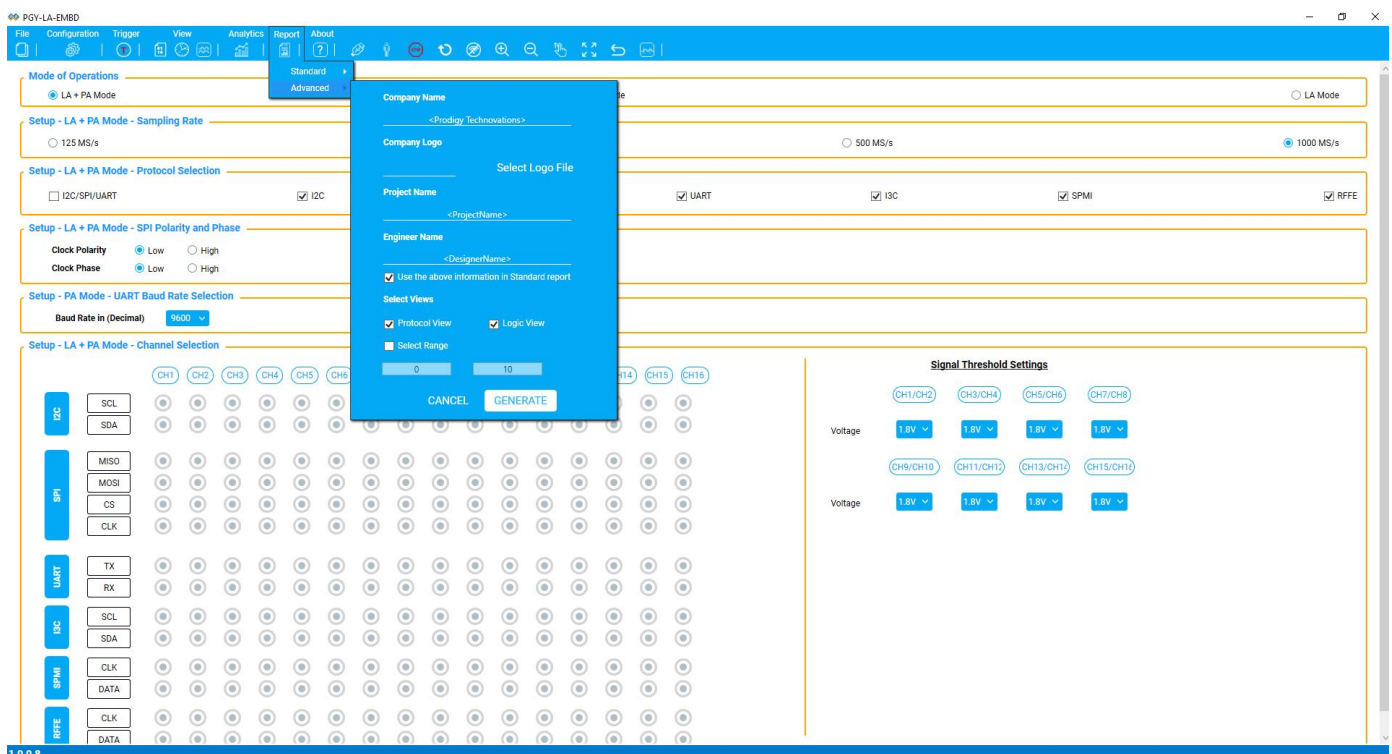
PGY-LA-EMBD supports Auto, Pattern, Protocol Aware and Timing Parameter trigger capabilities. Users can trigger on any of the Protocol packets. Comprehensive Trigger provides the flexibility to monitor different conditions.

Analytics

Detailed analytics on various protocols to enable better analysis and provide additional insights to designers

Report

Report can be generated in PDF or CSV format with details of all the signal information, plots and custom details like name of the company, logo, tester name, date and time to ensure designers can document all details and share the report.





PGY-LA-EMBD Specification

| Specifications | Features |
|--|---|
| No of Channels | 16 Logic Channels |
| State Speed | 100MHz (Synchronous Capture) |
| Timing Speed | 1GS/s (Asynchronous Capture) |
| Number of state clock support | Two, Flexibility to sample on rising or falling edge |
| Record Length | Smart Continuous streaming of data to HDD/SSD of host computer |
| Voltage Level Support | 0 to 5V with Flexibility to define logic threshold |
| Waveform Plot | Plots waveforms with flexible configurable bus diagram |
| Listing View | List all the data samples at each sampling point |
| Trigger for LA | Pattern Trigger, Pulse width trigger, Delay trigger |
| Protocol Decode Support | I2C, SPI, UART, I3C, SPMI and RFFE |
| Simultaneous decoding of I2C, SPI, UART | Yes , Connect I2C, SPI and UART bus to Logic Analyzer. Simultaneously captures the bus data and displays it in time correlated view with corresponding time waveforms. |
| Protocol View with timing view (PA+LA) | Displays the protocol decoded data with high sample rate and timing waveform at the same time |
| API Support | Support for Automation of Operation using Python and C++ |
| Connector type | Flying Lead Probe with Female Connectors #16 Micro Grabber Test Clips as Optional Accessories |
| External Triggers | Trigger Out SMA Connector |
| Markers | Six, with delta information between two markers. |

| | |
|-------------------|---|
| Views | Timing View State/Logic/Waveform Listing View Protocol View Bus-Diagram to display Protocol packets with timing diagram plot Auto Trigger – Default (Trigger on any packet) |
| Protocol Trigger | Pattern Trigger Protocol Aware Trigger- UART: Start bit, Parity Bit, Data SPI: MOSI Data, MISO data I2C: START bit, Address, Data, Address plus Data, ACK, NACK, Repeated START, STOP bit Timing parameter trigger: Pulse width (Positive or Negative) Delay Trigger |
| Capture duration | Smart streaming of Protocol Data to host HDD/SSD |
| Report | Report Generation in PDF and CSV format |
| Host Connectivity | USB 3.0 Type-C |
| Dimensions | 115mmx90mmx25mm |
| Weight | 300g |

Ordering Information

PGY-LA-EMBD (v 1.0): Logic Analyzer for Embedded Interfaces.

Deliverables for PGY-LA-EMBD

PGY-LA-EMBD Unit.

USB 3.0 cable.

5V DC Power Supply.

PGY-LA-EMBD Software in CD.

Flying lead probe cable with female connector to connect to DUT.

Optional Accessories

PGY-LA-EMBD-Cable: Flying lead probe cable with female connector to connect to DUT Micro Grabber Test Clips (#16 Nos).

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About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.