Protocol Exerciser and Analysis of Mainstream and Emerging serial bus technologies

Member of

contributing member of mipi alliance

JEDEC

SD Association

PCI SIG

Prodigy TECHNOVATIONS

Protocol Exerciser and Analysis of Mainstream and Emerging serial bus technologies

Prodigy Technovations - At a Glance

Prodigy Technovations is a leading global technology provider of protocol exercisers and analyzers for emerging and mainstream serial bus standards. Prodigy Technovations has successfully developed these products and deployed in top multibillion-dollar semiconductor companies for pre and post silicon validation. Over the last 13 years period Prodigy Technovations has developed deep expertise in electrical validation tools for physical layer electrical validation using the data captured by industry leading Tektronix oscilloscopes.

- Protocol Exercisers and Analyzer for leading edge technologies such as PCIe, UFS, eMMC, SD, SDIO, I3C, RFFE, SPMI, I2C and more.
- Probing solution for high-speed serial bus technologies for speeds up to 32Gbps.
- Decoding high speed serial bus packets in hardware.
- Developing algorithm to continuously capture and manage high speed data-logging.
- Analysis of very large amount of data for debugging design issues.
- Powerful hardware based protocol aware trigger capabilities to capture protocol specific events.

Prodigy Portfolio & Coverage

Protocol /Interface	Protocol Analyzer	Exerciser	Protocol Decode (Scope Based)	Electrical Validation (Scope Based)
I2C	✓	✓	✓	✓
SMBus	✓	✓		
PMBus	✓	✓		
I3C	✓	✓	✓	✓
UART	✓	✓	✓	✓
SPI	✓	✓	✓	✓
QSPI	✓	✓	✓	✓
eSPI	✓	✓	✓	
RFFE	✓	✓	✓	
SPMI	✓	✓	✓	✓
SMI (MDIO)	✓	✓		
JTAG	✓	✓	✓	
100BaseT1 (Automotive)	✓		✓	
eMMC	✓		✓	✓
SD	✓		✓	✓
SDIO	✓		✓	✓
UFS 4.0 (backward Compatible)	✓		✓	
UniPro			✓	
LLI			✓	
I2S	✓	✓	✓	✓
HSIC			✓	
DigRF v4			✓	
SSIC			✓	
ONFI v4				✓
PCIe Gen 3	✓			
PCIe Gen 4	✓			
USB PD, 3.1, 3.0, 2.0			✓	
HDMI, MHL			✓	
FlexRay			✓	

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UFS 4.0/3.1

Protocol Analyzer and Exerciser

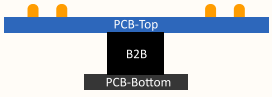
PGY-UFS4.0-PA, UFS Protocol Analyzer is the industry first working and tested UFS4.0 Protocol Analyzer. It offers protocol data capture and debug of data across MPHY, UniPro and UFS protocol layers. It allows for instantaneous decoding of UFS, UniPro and MPHY layers with flexibility to correlate decoded data across these protocol layers. PGY-UFS4.0-PA supports PWMG1 to HSG5B data rates and two TX, two RX lane decode. The active probe has minimum electrical loading on device under test (DUT) and captures protocol data without affecting the performance of DUT. PGY-UFS4.0-PA Protocol Analyzer support two lane data. Comprehensive on the fly decoding of UniPro & UFS data enables validation of communication between UFS host and device.

PGY-UFS4.0-PA Protocol Analyzer allows Design and Test Engineers to obtain deep insight into UFS host and device communication. MPHY/UniPRO/UFS packet-based triggering allows specific protocol data capture and analysis. PGY-UFS Protocol analyzer instantaneously provides decoding of UFS, UniPro and MPHY layers with a correlation to MPHY, UniPro and UFS layers.

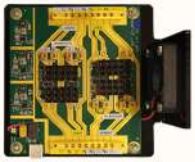
- Industry's first working UFS4.0 Protocol Analysis solution tested on real world DUT.
- Supports UniPro and UFS CTS
- Supports data rate upto HSG5B (23.32 Gbps data rate per lane).
- Protocol aware trigger capabilities at PACP, UniPro and UFS layer.
- Supports version MPHY 4.0, UniPro 1.8/2.0, and UFS v2.1/3.1/4.0.
- Supports PWM G1 to G7 and HS G 1, 2, 3, 4, 5 Rate A and B Series.

P4012 - HSG5B (23.32Gbps)
Solder-in probetips

UFS4.0 Compatible
CTLE Probe tips



P4012-INT-B2B
UFS 4.0 Board to
Board Interposer



mSMP Power divider
Interposer PCB
(with integrated probe tip)

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PCIe Gen3/4
Protocol Analyzer

The PGY-PCIeGen3/4-PA is a PCIe Protocol Analyzer that supports protocol analysis up to PCIe Gen4 speeds. PCIe design and test engineers can easily captures and record traces at 2.5, 5.0, 8 and 16GT/s at specific event and obtain error report instantaneously at affordable price. This enables the design and test engineers to reduce the development time and address the time to market needs. PCIe Gen4 data is captured using interposers between the root complex and end point (Device under test). PCIe Gen4 interposers support. PCIe Gen4 Protocol Analyzer's software provides complete decode and error analysis of Transaction Layer Packets (TLPs), data link Layer Packets and with LTSSM information.

- Supports PCIeGen3/4 data rate at X4 link.
- Supports M.2, U.2, AIC, CEM and Solder in probing solutions.
- 64GB memory Depth.
- Powerful trigger capabilities.
- Protocol Analysis Software.

PGY-INT-M.2 : Prodigy M.2 Interposer

PGY-INT-SDX – Prodigy
SD Express Interposer

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HIGH SPEED PROTOCOL & INTERFACES

eMMC (HS400), SD (UHS-I), SDIO (UHS-I) and UHS II Protocol Analyzer

- Analysis of CMD CRC errors, Response CRC errors, Data CRC errors, Timing Values, and Reserved commands.
- Hardware-based protocol-aware trigger capability in real-time enables capturing specific events.
- Probing Solution to support different DUT.
- Continuous streaming of Protocol data.
- Protocol analysis for eMMC(HS400), SD(UHS-I), SDIO(UHS-I) and UHS-II Speeds.

100baseT1 Automotive Ethernet Protocol Analyzer

- Passive tapping allows non-intrusive method of monitoring 100BASE-T1 Bus.
- Powerful multi-layer protocol layer trigger capabilities enable capturing data at specific events.
- Decoding of TC10 Sleep and Wakeup events of master and slave.
- Continuous streaming provides unlimited capture of 100BASE-T1 signals.

QSPI Protocol Exerciser and Analyzer

- Supports QSPI speeds of up to 80MHz.
- Extended, Dual and Quad QSPI Modes Supported.
- Continuous streaming provides unlimited protocol capture of QSPI signals.
- STR and DTR Transfer rates.
- API support for automation in Python and C++.

SD eMMC AC/DC Tester

- Supports eMMC 4.41, 4.51, 5.0, 5.1 and SD card 2.0/3.0 (UHS-I) Specifications.
- Supports host controller for eMMC and SD card and flexibility to place devices in operating modes.
- Exerciser capability to write different test cases and inject the traffic to devices.
- Controls the eMMC and SD card host controller and oscilloscope signal acquisition for seamless measurement analysis.
- Provides all AC/DC measurements and generates detail report.

LOW SPEED PROTOCOL & INTERFACES

I3C Protocol Exerciser and Analyzer

- Frequency range from 1Hz-12.5MHz.
- Variable voltage levels from 0.9V – 3.4V in steps of 5mV.
- Only vendor in the market with CTS v1.1 support.
- Setup and hold variation in steps of 18ps.
- Protocol level error injection.
- Can be used as sniffer in streaming mode.

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I2C/SPI Protocol Exerciser and Analyzers

- Variable voltage levels from 0.9V – 3.4V in steps of 30mV.
- Frequency range up to 50MHz.
- Timing parameter variation.
- Ability to configure the device as Master/Slave.
- Protocol layer error injection.
- Trigger capabilities.
- Can be used as sniffer in streaming mode.

SPMI Protocol Exerciser and Analyzer

- Supports SPMI v1.0/v2.0 Specifications.
- Frequency Level support from 32KHz-26MHz.
- Supports Request Capable Slave (RCS) feature and complex BUS arbitration process.
- Timing and Amplitude parameter variation.
- Supports Protocol conformance Implementation Suite (Test cases as per MIPI Alliance Spec)

RFFE Protocol Exerciser and Analyzer

- Supports RFFE 2.0/2.1 Specifications.
- SCL frequency support from 32KHz-52MHz.
- Amplitude and timing variations.
- Can be used as sniffer and stream the protocol data for analysis.
- Supports Protocol conformance Implementation Suite (Test cases as per MIPI Alliance Spec).

UART Protocol Exerciser and Analyzers

- Supports custom UART traffic generation.
- Simultaneously generate UART traffic and Protocol decode of the bus.
- Variable UART baud rates.
- Continuous streaming of protocol data to the host computer to provide a large buffer.
- A timing diagram of Protocol decoded bus.

JTAG Protocol Exerciser and Analyzer

- Supports JTAG frequencies of up to 25MH.
- Simultaneously generate JTAG traffic and Protocol decode of the bus.
- JTAG Master Capability.
- Variable JTAG Data speeds and Duty cycle.
- User-defined TCK & TDI Delays.
- Continuous streaming of protocol data to the host computer to provide a large buffer.

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SMBus Protocol Exerciser and Analyzer

- Supports SMBus 3.4Mbps Speed.
- Ability to configure it as Master or Slave.
- Simultaneously generate SMBus traffic and Protocol decode of the bus.
- SMBus Master and Slaves.
- Error Injection ACK/NACK errors.
- Variable SMBus data speeds and duty cycle.
- Continuous streaming of protocol data to the host computer to provide large buffer.

PMBus Protocol Exerciser and Analyzer

- Supports PMBus Specifications.
- Ability to configure it as Master/Slave.
- Variable data speeds.
- Generate PMbus traffic and protocol decode of the bus.
- A timing diagram of the protocol decoded bus.
- Ability to write exerciser script to combine multiple frame generation at different data speeds.

MDIO Protocol Exerciser and Analyzer

- Supports MDIO speeds of up to 25MHz.
- Ability to configure it as Master or Slave.
- Simultaneously generate MDIO traffic and Protocol decode of the bus.
- MDIO Master and Slaves.
- Support for MDIO Clause 22 & 45.
- Variable MDIO data speeds and Duty cycle.

16 Ch, 1Gs/sec Logic Analyzer

- 16 channels with Protocol and Logic Analysis capability.
- 1GS/Sec Timing (Asynchronous) Analysis.
- Powerful trigger protocol aware trigger capabilities.
- 100MHz State (Synchronous) Analysis.
- Protocol Analysis of I2C-SPI-UART-I3C-SPMI-CAN/CAN FD and RFFE.
- Continuous streaming provides unlimited protocol capture.

SCOPE BASED ELECTRICAL VALIDATION AND PROTOCOL DECODE SOFTWARES

- Imports oscilloscope acquired data for electrical validation and protocol decode.
- Simultaneous protocol decode and electrical measurements.
- Supports live analysis of data captured by Tektronix Oscilloscope.
- Offline support for H5 and trc file format for other vendor oscilloscope.
- Supports I2C, SPI, UART, I3C, SPMI, RFFE, eMMC, SD, SDIO, USB2/0/3.0/3.1/3.2, UFS and many more.

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Prodigy TECHNOVATIONS

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